AF

PATENT

Case Docket No. ASMEX.320A
Date: January 12, 2005

In re application of	:	Pomarede et al.
Appl. No.	:	10/074,722
Filed	:	February 11, 2002
For	:	INTEGRATION OF HIGH K GATE DIELECTRIC
Examiner	:	Ron Everett Pompey
Art Unit	:	2812

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Joseph J. Mallon, Reg. No. 39,287

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Pomarede et al.
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CERTIFICATE OF MAILING

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Further to the Notice of Appeal submitted to the Office on November 15, 2004, Appellants hereby submit this Appeal Brief and the required fee pursuant to 37 C.F.R. § 41.37. The Honorable Board of Patent Appeals and Interferences has jurisdiction over this appeal pursuant to 35 U.S.C. § 134.

REAL PARTY IN INTEREST

ASM America, Inc. is the assignee of the above-captioned patent application and the real party in interest in this appeal.

RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative, and the assignee of the above-captioned patent application are unaware of any prior or pending appeals, interferences or judicial proceedings that are related to, that directly affect or would be directly affected by, or that would have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-9, 13-20, 22-27 and 29-47 are pending in this application and stand rejected. The grounds for rejecting each of Claims 1-9, 13-20, 22-27 and 29-47 are summarized below under the section heading entitled "Grounds of Rejection to be Reviewed on Appeal."

STATUS OF AMENDMENTS

The claims were not amended after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The independent claims subject to this appeal are Claims 1, 20, and 33. Pursuant to 37 C.F.R. § 41.37, a concise explanation of the subject matter defined in each of the independent claims is provided below (organized in the form of a Background subsection pertaining in a general way to all of the pending claims and additional subsections corresponding to each independent claim). Since the specification contains paragraph numbers pursuant to 37 C.F.R. § 1.52(b)(6) (instead of line numbers), the concise explanations provided below refer to various portions of the specification by paragraph number.

Background

The inventions of independent Claims 1, 20 and 33 relate generally to forming semiconductor layers in integrated circuit fabrication, and more particularly to forming gate electrodes over high dielectric constant ("high k") gate dielectrics in a transistor gate stack. *See* paragraph 0002 at 1. As is known in the art, a transistor typically includes a gate electrode separated from a semiconductor layer or substrate by a thin gate dielectric material. *See* paragraph 0004 at 1. Conventional gate electrodes are formed of polysilicon doped with conductivity-enhancing impurities, such as arsenic, phosphorus or boron. Such doped polysilicon gate electrodes can be deposited by chemical vapor deposition ("CVD") with *in situ* doping by flowing a dopant source gas (*e.g.*, arsine, phosphine, diborane, etc.) concurrently with a silicon source gas (*e.g.* silane). *See* paragraph 0005 at 1. Gate electrodes may also be formed of silicon germanium ("SiGe"), *e.g.*, by CVD using germane (GeH_4) along with silane (SiH_4). *See* paragraph 0006 at 1-2. These gate electrodes may be formed over traditional dielectric materials such as silicon dioxide or high dielectric constant materials such as silicon nitride

(Si_3N_4), aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), hafnium oxide (HfO_2), barium strontium titanate (BST), strontium bismuth tantalate (SBT), tantalum oxide (Ta_2O_5), etc. *See* paragraph 00015 at 4.

However, it has been found that gate electrode materials (such as polysilicon and SiGe) tend to nucleate poorly over dielectric materials. *See* paragraph 0007 at 2. Slow nucleation entails longer overall deposition times, lower throughput and consequently greater fabrication costs. *See* paragraph 0008 at 2. One way in which SiGe or other *in situ* doped silicon deposition has been hastened is by the first formation of a nucleation layer, typically silicon, over the gate dielectric, followed by *in situ* doped deposition (of, *e.g.*, SiGe or electrically doped silicon). *See* paragraph 0010 at 2. However, this additional step complicates the process flow and requires adjustment of the doping concentrations at the dielectric-electrode interface to ensure the desired work function for the transistor. *See* paragraph 0010 at 2 and paragraph 0017 at 4. Accordingly, a need exists for improvements in the integration of dielectric layers and conductors in semiconductor fabrication, particularly at interfaces in transistor gate stacks. *See* paragraph 0018 at 4.

The present invention provides methods for improving deposition over high k materials. *See* paragraph 0019 at 5. The inventors have found that traditional methods of depositing silicon-containing materials, such as polysilicon and poly-SiGe, over high k dielectrics tend to results in poor electrical performance of resultant devices. *See* paragraph 0020 at 5. One possible reason for this poor performance identified by the inventors is the reduction of oxides. *See* paragraph 0020 at 5. Accordingly, processes are provided for depositing electrode materials, preferably silicon-containing layers, over high k materials while minimizing reduction of the high k materials. *See* paragraph 0021 at 5. At least during an initial seed phase, deposition conditions are arranged to minimize diffusion of hydrogen to the high k material. *See* paragraph 0021 at 5. Preferably, a second or bulk phase of deposition includes altered conditions arranged to increase the deposition rate such that overall throughput for the deposition is not excessively affected. *See* paragraph 0021 at 5.

Claim 1

Independent Claim 1 recites:

1. A method of forming a transistor gate stack, comprising:

forming a high dielectric constant material over a semiconductor substrate;

depositing a silicon-containing seed layer over the high dielectric constant material under seed phase conditions comprising flowing trisilane; and

depositing a silicon-containing bulk layer over the seed layer under bulk phase conditions different from the seed phase conditions, the bulk phase conditions selected to result in a higher deposition rate than the seed phase conditions.

The claimed method is described in the specification at, *e.g.*, paragraph 0022 (page 5) and paragraph 0057 (page 13, use of trisilane). Embodiments of the claimed method are disclosed throughout the specification. For example, Figure 2 shows a general process sequence in accordance with the invention, illustrated in the context of forming a transistor gate stack on a semiconductor substrate. *See* paragraph 0058 (pages 13-14). The formation 70 of a high dielectric constant material over a semiconductor substrate is described in, *e.g.*, paragraphs 0060 to 0074 (pages 14 to 18). Arrangement of the seed phase conditions at step 74 to minimize hydrogen reduction by using trisilane as a deposition gas is described in, *e.g.*, paragraphs 0077 to 0078 (pages 18-19). Deposition of the silicon-containing seed layer 74 and silicon-containing bulk layer 78 is described in, *e.g.*, paragraphs 0075 to 0076 (page 18) and 0079 to 0089 (pages 19-22).

Claim 20

Independent Claim 20 recites:

20. A method of forming a structure in an integrated circuit, comprising:

forming a layer of high dielectric constant material; and

depositing an electrode material over the layer of high dielectric constant material by flowing a silicon source gas comprising trisilane.

The claimed method is described in the specification at, *e.g.*, paragraph 0023 (pages 5-6) and paragraph 0057 (page 13, use of trisilane to minimize hydrogen content). Embodiments of the claimed method are disclosed throughout the specification. For example, Figures 8-14 are reproductions of scanning electron micrographs of gate electrode layers deposited over high

dielectric constant materials by flowing a silicon source gas comprising trisilane as described in, *e.g.*, paragraphs 0033 (page 6) and 0102 to 0104 (pages 24-25).

Claim 33

Independent Claim 33 recites:

33. A method of forming a silicon-containing material over a high dielectric constant material, comprising:

loading a substrate into a single-substrate reaction chamber;

depositing a silicon-containing layer over a high dielectric constant layer on the substrate by flowing a silicon source gas comprising trisilane without flowing hydrogen.

The claimed method is described in the specification at, *e.g.*, paragraph 0024 (page 6) and paragraph 0057 (page 13, use of trisilane). Embodiments of the claimed method are disclosed throughout the specification. For example, loading of a substrate into a single-substrate reaction chamber is described in, *e.g.*, paragraph 0063 (pages 15-16). Figures 8-14 are reproductions of scanning electron micrographs of gate electrode layers deposited over high dielectric constant materials by flowing a silicon source gas comprising trisilane as described in, *e.g.*, paragraphs 0033 (page 6) and 0102 to 0104 (pages 24-25). Minimization or elimination of hydrogen from the deposition on the high-k material is described in, *e.g.*, paragraphs 0024 (page 6) and 0077 to 0078 (pages 18-19).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Examiner finally rejected Claims 1-9, 13-20, 22-27 and 29-47 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,373,112 to Murthy et al. ("Murthy") in view of U.S. Patent No. 6,319,782 to Nakabayashi et al. ("Nakabayashi") and U.S. Patent No. 5,879,970 to Shiota et al. ("Shiota").

ARGUMENTS

Appellants provide the following arguments in support of the patentability of Claims 1-9, 13-20, 22-27 and 29-47. Independent Claims 1 and 20 are argued together, separately from independent Claim 33 (under separate subheadings, along with their corresponding dependent

claims) and thus do not stand or fall together. *See* 37 C.F.R. 41.37(c)(vii) ("Any claim argued separately should be placed under a subheading identifying the claim by number).

I. The Examiner erred by finally rejecting Claims 1-9, 13-20, 22-27, 29-32 and 40-41 under 35 U.S.C. § 103(a) as being unpatentable over Murthy in view of Nakabayashi and Shiota.

The Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness.

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references combined) must teach or suggest all the claim limitations.

M.P.E.P. § 2142. For the reasons set forth below, Appellants respectfully submit that the Examiner has failed to establish a *prima facie* case of nonobviousness. Therefore, Appellants respectfully request reversal of the rejection of Claims 1-9, 13-20, 22-27, 29-32 and 40-41 under 35 U.S.C. § 103(a) as being unpatentable over Murthy in view of Nakabayashi and Shiota.

A. There is no motivation to combine Murthy with Nakabayashi and Shiota.

The Examiner characterizes the primary reference, Murthy, as follows:

> Murthy discloses the limitations of claims 1-47:
> depositing a silicon-containing seed layer (106, fig. 2) over the high dielectric constant material (104, fig. 2) under seed phase conditions (col. 2, lns. 29-38); and
> depositing a silicon-containing bulk layer (108, fig. 2) over the seed layer under bulk phase conditions, the bulk phase conditions selected to result in a higher deposition rate than the seed phase conditions (col. 4, ln. 41 – col. [5], line 9).

Final Office Action mailed 10/5/04 at 2. Appellants note that Claims 1-9, 13-20, 22-27, 29-32 and 40-41 were not rejected under 35 U.S.C. § 102, the Examiner apparently recognizing that none of the cited references disclose all of the limitations recited in each of the claims. Each of Claims 1-9, 13-20, 22-27, 29-32 and 40-41 recite a combination of limitations, including the use of trisilane. Murthy deposits the seed film using SiH_4, *see* Murthy col. 4, line 55, not trisilane as

claimed, and thus the Examiner apparently recognizes that Murthy does not disclose the use of trisilane.

The Final Office Action continues as follows:

> Murthy discloses the claimed limitations, as described above, except for the limitations disclosed below by Nakabayashi and Shiota:
>
> Nakabayashi discloses:
>
> using a non-hydrogen carrier gas; and
>
> wherein the seed phase is less than 500 Å/min and the deposition rate for of [sic] the bulk phase is greater than 500 Å/min (col. 10, ln. 44 – col. 11, ln. 31);
>
> Shiota discloses:
>
> using a non-hydrogen carrier gas (col. 1, lns. 20-40); and
>
> **wherein trisilane is used as a silane gas** (col. 1, lns. 20-40);
>
> Therefore one of ordinary skill would have combined the limitations disclosed in Nakabayashi and Shiota with Murthy, because the non-hydrogen carrier gases can remove/reduce unwanted oxides and that it is conventional to form silicon or silicon germanium layers whether with hydrogen or non-hydrogen carrier gases.

Final Office Action mailed 10/5/04 at 2-3 (emphasis added). The Examiner states that "Shiota discloses, '. . . silane, which is expressed as $Si_n H_{2n+2}$ where n is an integer between 1 and 3. . .'. Therefore, one of ordinary skill would use any one of these three compositions of silane to form a silicon seed layer." Final Office Action mailed 10/5/04 at 3.

However, the Examiner does not say why the skilled artisan "would use any one of these three compositions of silane to form a silicon seed layer." *Id.* As noted above, Murthy discloses the use of SiH_4, not trisilane. The Examiner has failed to allege a motivation for modifying Murthy to replace SiH_4 with trisilane. Therefore, the motivation alleged by the Examiner fails to support a *prima facie* case of obviousness because it is only directed to what one skilled in the art could do, not to what one would do: "Fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish *prima facie* obviousness." M.P.E.P. § 2143.01.

B. Modifying Murthy by replacing hydrogen with Nakabayashi's chlorine would render Murthy's gate oxide unsuitable for its intended purpose.

"If proposed modification would render the prior art invention being modified unsuitable for its intended purpose, then there is no suggestion or motivation to make the proposed modification." M.P.E.P § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984)).

Murthy discloses depositing silicon-containing layers using flowing hydrogen (H_2) as a carrier gas. *See* Murthy at col. 4, lines 52-63 and col. 5, line 5. The motivation asserted by the Examiner for combining the cited references focuses on the use of non-hydrogen carrier gases: "Therefore, one of ordinary skill would have combined the limitations disclosed in Nakabayashi and Shiota with Murthy, because **the non-hydrogen carrier gases can remove/reduce unwanted oxides** and that it is conventional to form silicon or silicon germanium layers whether with hydrogen or non-hydrogen carrier gases." Final Office Action mailed 10/5/04 at 3 (emphasis added). In particular, the Examiner cites Nakabayashi's use of chlorine gas: "Nakabayashi (col. 10, lns. 44-47; 51-55) discloses using Chlorine as a carrier gas, **to strip away unwanted oxide** that is formed on silicon oxide film (see Nakabayashi, col. 10, lns. 52-54)." Office Action mailed 5/3/04 at 3 (emphasis added). Thus, the Examiner's position appears to be that the disclosure of non-hydrogen carrier gases by the secondary references (Shiota and Nakabayashi) would motivate one skilled in the art to modify the primary reference (Murthy) to replace the hydrogen carrier gas with a gas such as chlorine in order to "remove/reduce unwanted oxides." *Id.*

However, the Examiner has failed to identify any such "unwanted oxides" in Murthy. To the contrary, Murthy desires an "ultra- thin" high quality gate oxide substrate, *see* Murthy at col. 3, lines 43-60, and thus does not desire the removal of oxides or consider them to be "unwanted." Murthy uses a gate oxide 104 as a substrate for the deposition of the Si layer 106, *see* Murthy at col. 4, lines 52-56. The gate oxide is a necessary component of Murthy's MOFSET structure, *see* Murthy at col. 4, lines 7-20 and Figure 5. Murthy's gate oxide is extremely thin ("gate oxide 104 is approximately 15 angstroms thick," *see* Murthy at col. 4, lines 18-19) and thus Murthy's process is designed to prevent destruction of the ultra-thin gate oxide during subsequent deposition ("the gate oxide quality is not significantly degraded by processes embodying the present invention . . .", *see* Murthy at col. 3, lines 65-67). The replacement of Murthy's hydrogen carrier gas with chlorine in the manner indicated by the Examiner would likely remove or seriously degrade the ultra-thin oxide layer, thereby rendering Murthy's MOFSET structure unsuitable for its intended purpose. The Examiner admits that Nakabayashi's chlorine would "strip away unwanted oxide," Office Action mailed 5/3/04 at 3, but has failed to identify any such "unwanted oxide" in Murthy. Even if such unwanted oxide did exist, there is no indication that the chlorine would somehow remove only the "unwanted" oxide without also attacking the

desired ultra-thin gate oxide. Therefore, there is no suggestion or motivation to combine Murthy with Shiota and Nakabayashi because the modification asserted by the Examiner would render Murthy unsuitable for its intended purpose.

C. <u>There is no reasonable expectation that Murthy could be successfully combined with Nakabayashi and Shiota.</u>

Murthy teaches deposition of a seed film using SiH_4 at a temperature between approximately 600 - 675°C. *See* Murthy col. 4, lines 52-65. Murthy teaches the desirability of a "very thin and highly nanocrystalline seed film," see col. 4, lines 58-60, and a seed film that "substantially prevents exposure of the gate oxide to gas mixtures containing GeH_4," see col. 3 line 67 to col. 4 lines 1-2. Thus, Murthy teaches the desirability of forming a highly uniform seed film.

Shiota discloses trisilane, but teaches that Murthy's deposition temperatures are undesirable: "On the other hand, when the substrate temperature exceeds 600 degrees in centigrade, the material gas is decomposed, and **the thin film is not uniform in quality**." Shiota col. 1, lines 37-40 (emphasis added). Thus, one skilled in the art would not reasonably expect to be able to produce high quality thin film by modifying Murthy's process to include trisilane because Shiota teaches away from the use of trisilane at Murthy's deposition temperatures.

II. <u>The Examiner erred by finally rejecting Claims 33-39 and 45-47 under 35 U.S.C. § 103(a) as being unpatentable over Murthy in view of Nakabayashi and Shiota</u>.

Appellants note that Claims 33-39 and 45-47 were not rejected under 35 U.S.C. § 102, the Examiner apparently recognizing that none of the cited references disclose all of the limitations recited in each of the claims.

For the reasons set forth below, Appellants respectfully submit that the Examiner has failed to establish a *prima facie* case of nonobviousness. Therefore, Appellants respectfully request reversal of the rejection of Claims 33-39 and 45-47 under 35 U.S.C. § 103(a) as being unpatentable over Murthy in view of Nakabayashi and Shiota.

A. <u>None of the cited references teach or suggest depositing a silicon-containing layer "without flowing hydrogen" as claimed</u>.

Each of Claims 33-39 and 45-47 recite a combination of limitations, including depositing a silicon-containing layer without flowing hydrogen. As noted above, Murthy discloses depositing silicon-containing layers using flowing hydrogen (H_2) as a carrier gas. *See* Murthy at col. 4, lines 52-63 and col. 5, line 5. Shiota also discloses the use of a hydrogen carrier gas. *See* Shiota at col.6, lines 17-18.

None of the asserted references teach or suggest that depositing without flowing hydrogen is particularly desirable. However, the Examiner has taken the position that the mere disclosure of other carrier and reactant gases would motivate one skilled in the art to conduct Murthy's process without flowing hydrogen:

> Therefore one of ordinary skill would have combined the limitations disclosed in Nakabayashi and Shiota with Murthy, because the non-hydrogen carrier gases can remove/reduce unwanted oxides and that it is conventional to form silicon or silicon germanium layers whether with hydrogen or non-hydrogen carrier gases.

Final Office Action mailed 10/5/04 at 2-3 (emphasis added). However, Shiota and Nakabayashi do not exclude the possibility that mixtures of such non-hydrogen gases with hydrogen could be used for depositions, nor teach the desirability of using any particular gas in the absence of another, let alone without flowing hydrogen. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness because the cited references neither teach nor suggest "without flowing hydrogen" as claimed.

B. Shiota teaches away from depositing "without flowing hydrogen" as claimed.

Shiota specifically teaches the desirability of depositing with hydrogen: "When hydrogen was used as the dilution gas, crystal defects at the grain boundaries were cured by the hydrogen. Thus, the hydrogen achieved a high quality polycrystalline silicon-germanium alloy layer." Shiota at column 4, lines 44-47. Rather than establishing a motivation to combine, Shiota teaches away from the instantly claimed combinations of limitations.

C. There is no motivation to combine Murthy with Nakabayashi and Shiota.

For reasons similar to those argued separately in Section I.A above (and hereby incorporated into this subsection by reference), the Examiner has failed to allege a motivation modify Murthy to replace SiH_4 with trisilane. The Examiner's allegation that "one of ordinary skill would use any one of these three compositions of silane to form a silicon seed layer," Final

Office Action mailed 10/5/04 at 3, is only directed to what one could do, not what one would do. "Fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish *prima facie* obviousness." M.P.E.P. § 2143.01. In addition, for reasons similar to those argued separately in Section I.B above (and hereby incorporated into this subsection by reference), there is no motivation to modify Murthy by replacing the hydrogen carrier gas with Nakabayashi's chlorine in the manner indicated by the Examiner because the chlorine would degrade Murthy's gate oxide and thereby render it unsuitable for its intended purpose.

D. <u>There is no reasonable expectation that Murthy could be successfully combined with Nakabayashi and Shiota.</u>

For reasons similar to those argued separately in Section I.C above (and hereby incorporated into this subsection by reference), one skilled in the art would not reasonably expect to be able to produce high quality thin film by modifying Murthy's process to include trisilane because Shiota teaches away from the use of trisilane at Murthy's deposition temperatures.

CONCLUSION

For the reasons discussed above, Appellants respectfully request that the Honorable Board reverse all of the outstanding rejections of the pending claims. The undersigned may be contacted at the telephone number provided below with any questions regarding this application.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 1/12/05

By: Joseph J. Mallon

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CLAIMS APPENDIX

1. A method of forming a transistor gate stack, comprising:

forming a high dielectric constant material over a semiconductor substrate;

depositing a silicon-containing seed layer over the high dielectric constant material under seed phase conditions comprising flowing trisilane; and

depositing a silicon-containing bulk layer over the seed layer under bulk phase conditions different from the seed phase conditions, the bulk phase conditions selected to result in a higher deposition rate than the seed phase conditions.

2. The method of Claim 1, wherein a deposition rate of the seed phase conditions is less than 500 Å/min and the deposition rate of the bulk phase conditions is greater than 500 Å/min.

3. The method of Claim 2, wherein the deposition rate of the seed phase conditions is between about 10 Å/min and 100 Å/min.

4. The method of Claim 1, wherein the seed phase conditions include a lower temperature than the bulk phase conditions.

5. The method of Claim 1, wherein the seed phase conditions include a lower partial pressure than the bulk phase conditions.

6. The method of Claim 1, wherein the seed phase conditions include supplying a non-hydrogen carrier gas with the trisilane.

7. The method of Claim 6, wherein the bulk phase conditions include supplying a non-hydrogen carrier gas with a silicon source gas.

8. The method of Claim 1, wherein the seed layer and the bulk layer form a silicon-germanium gate stack.

9. The method of Claim 1, wherein the bulk layer is *in situ* electrically doped.

10. Canceled

11. Canceled

12. Canceled

13. The method of Claim 1, wherein depositing comprises heating the substrate to a temperature between about 400°C and 600°C.

14. The method of Claim 1, wherein the partial pressure of the trisilane in the seed phase conditions is between about 1 mTorr and 1 Torr.

15. The method of Claim 14, wherein the seed phase conditions include flowing an inert, non-hydrogenated carrier gas.

16. The method of Claim 15, wherein the carrier gas comprises nitrogen.

17. The method of Claim 15, wherein the bulk phase conditions also comprise flowing the inert, non-hydrogenated carrier gas.

18. The method of Claim 1, wherein the high dielectric constant material is selected from the group consisting of zirconium oxide, hafnium oxide, tantalum oxide, aluminum oxide, barium strontium titanate, strontium bismuth tantalate, and lanthanide oxides.

19. The method of Claim 18, wherein the high dielectric constant material comprises zirconium oxide.

20. A method of forming a structure in an integrated circuit, comprising:

forming a layer of high dielectric constant material; and

depositing an electrode material over the layer of high dielectric constant material by flowing a silicon source gas comprising trisilane.

21. Canceled

22. The method of Claim 20, wherein depositing the electrode material further comprises flowing a germanium source gas.

23. The method of Claim 20, wherein depositing comprises maintaining a reaction chamber pressure between about 1 Torr and 100 Torr.

24. The method of Claim 23, wherein the reaction chamber pressure is maintained between about 10 Torr and 80 Torr.

25. The method of Claim 20, wherein depositing comprises maintaining a substrate temperature between about 300°C and 650°C.

26. The method of Claim 25, wherein the substrate temperature is maintained between about 400°C and 600°C.

27. The method of Claim 26, wherein the substrate temperature is maintained between about 450°C and 575°C.

28. Canceled

29. The method of Claim 20, wherein forming the layer of high dielectric constant material comprises an atomic layer deposition process.

30. The method of Claim 29, wherein the high dielectric constant material is selected from the group consisting of zirconium oxide, hafnium oxide, tantalum oxide, aluminum oxide, barium strontium titanate, strontium bismuth tantalate, and lanthanide oxides.

31. The method of Claim 29, wherein the high dielectric constant material comprises a mixture of metal oxides.

32. The method of Claim 31, wherein the mixture comprises hafnium oxide and aluminum oxide.

33. A method of forming a silicon-containing material over a high dielectric constant material, comprising:

loading a substrate into a single-substrate reaction chamber;

depositing a silicon-containing layer over a high dielectric constant layer on the substrate by flowing a silicon source gas comprising trisilane without flowing hydrogen.

34. The method of Claim 33, wherein depositing comprises a seed phase conducted at a first temperature and a bulk phase conducted at a higher temperature.

35. The method of Claim 34, wherein the seed phase comprises maintaining a temperature of the substrate between about 400°C and 650°C.

36. The method of Claim 33, wherein depositing comprises flowing nitrogen as a carrier gas for the silicon source gas.

37. The method of Claim 36, wherein the silicon source gas further comprises silane.

38. The method of Claim 33, wherein depositing comprises flowing a carrier gas comprising a noble gas along with the silicon source gas.

39. The method of Claim 33, wherein depositing comprises maintaining a temperature between about 300°C and 800°C.

40. The method of Claim 1, wherein the high dielectric constant material is a metal oxide.

41. The method of Claim 1, wherein the high dielectric constant material is a lanthanide oxide.

42. The method of Claim 20, wherein the high dielectric constant material is selected from the group consisting of zirconium oxide, hafnium oxide, tantalum oxide, aluminum oxide, barium strontium titanate, strontium bismuth tantalate, and lanthanide oxides.

43. The method of Claim 20, wherein the high dielectric constant material is a metal oxide.

44. The method of Claim 20, wherein the high dielectric constant material is a lanthanide oxide.

45. The method of Claim 33, wherein the high dielectric constant material is selected from the group consisting of zirconium oxide, hafnium oxide, tantalum oxide, aluminum oxide, barium strontium titanate, strontium bismuth tantalate, and lanthanide oxides.

46. The method of Claim 33, wherein the high dielectric constant material is a metal oxide.

47. The method of Claim 33, wherein the high dielectric constant material is a lanthanide oxide.